ABSTRACT OF THE DISCLOSURE

As a power-supply voltage VCC is applied to a second terminal, a latch is reset by a reset signal POR from a power-on reset unit. Subsequently, as the voltage of a signal IN applied to a first terminal is increased to higher than the voltage VCC by a threshold voltage Vth of a PMOS 11, the PMOS 11 turns on, causing a node N1 to become "H." Thus, a test mode is set in the latch. Subsequently, even if the signal IN is reduced to VCC or lower, the test mode is maintained. A high-voltage test can be conducted by increasing the power-supply voltage at the second terminal, thereby eliminating the need for applying the first terminal with a higher voltage than required to set the test mode. It is therefore possible to prevent a gate oxide film of a buffer from being destroyed.